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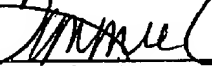|			
Applicant:	Jiang	Docket No:	TI-32309
Serial No:	09/828,116	Examiner:	Grier, Laura A.
Filed:	4/6/2001	Art Unit:	2644
For:	AN EFFICIENT DIGITAL AUDIO AUTOMATIC GAIN CONTROL		

APPEAL BRIEF PURSUANT TO 1.192(c)

Assistant Commissioner for Patents

Washington, DC   20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the final Office Action mailed August 17, 2005, and the Advisory Action mailed December 15, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-33 were originally filed, and Claims 1, 2, 5, and 23-24 have been cancelled.

Furthermore, Claims 8, 9, 12-14, 16-22, 29-30, 32, and 33 have either been indicated as allowable or as allowed.

Consequently, the subject of the instant appeal is Claims 3, 4, 6, 7, 10, 15, 25-28, and 31.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-33.

A Response After Final was filed on November 17, 2005, amending no claims.

The Advisory Action indicated that the request for consideration had been considered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

System aspects of the new digital AGC will first be described, followed by two design examples to elaborate more details of the new digital AGC.

A diagram of a new AGC design is shown in Figure 1 at 10 where the main blocks are described as follows:

ROM_CSD (M x L-bits): table storing CSD codes (based on actual gain values).

ADDR_A (n-bits): address register pointing to ROM_CSD.

REG_A (K-bits): register having the lower SPL value.

COMP_A (K-bits): comparator with two inputs - peak_input and REG_A.

ROM_SPL (N x K-bits): table storing SPL values.

ADDR_B (n-bits): address register pointing to ROM_SPL.

REG_B (K-bits): register having the upper SPL value.

COMP_B (K-bits): comparator with two inputs – peak_input and REG_B.

CSD_MULTIPLY: CSD gain multiplier.

The main components of the new AGC are detailed and show how these parameters M, N(n), K and L are related and selected as follows:

The State Machine

The state machine consists of two comparators COMP_A, COMP_B and registers REG_A, REG_B, ADDR_A and ADDR_B, and its procedure is quite straightforward. The peak input, always a positive number, is a measure of the peak level of the input signal. Comparator COMP_A compares the peak input and the content of register REG_A, and comparator COMP_B compares the peak input and the content of register ADDR_B. There are three cases the state machine adjusts accordingly:

Case 1: REG_B > peak_input $\geq$ REG_A. In this case no changes are enacted in any registers of the state machine.

Case 2: peak_input < REG_A. Then the following adjustments proceed:

move (content of) REG_A into REG_B;

move ADDR_A into ADDR_B;

decrease ADDR_A by 1;

ADDR_A obtains the SPL value pointed by the new ADDR_A;

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Case 3: peak_input $\geq$ REG_B. The following updates are made:

move REG_B into REG_A;

move ADDR_B into ADDR_A;

increase ADDR_B by 1;

Register ADDR_B obtains the SPL value pointed by the new ADDR_B;

Note that register ADDR_A's content minus one is the address that always points to the current gain value (CSD code) in ROM_CSD.

It is noted that register ADDR_B could be dropped since its content is just an increment of one over the content of ADDR_A. An up-counter and a multiplexer circuit can be added to obtain the correct value going into ROM_SPL. Using register ADDR_B makes the description of the state machine function more straightforward.

AGC Hysteresis

Hysteresis may be added to the digital AGC by adding a variable offset to the ROM_CSD address.

new ROM_CSD address = original ROM_CSD address + OFFSET

For P+Q steps of hysteresis the offset may be determined by augmenting the AGC state machine as follows (as corresponding, additional statements to those of the previous three cases):

Case 1: If register ADDR_A is at its maximum (minimum) value and

OFFSET is not 0, increment(decrement) OFFSET. Otherwise, leave OFFSET unchanged.

Case 2: If OFFSET < P, increment OFFSET. Otherwise, leave OFFSET unchanged.

Case 3: If OFFSET > -Q, decrement OFFSET. Otherwise, leave OFFSET unchanged.

With this method, the actual AGC gain with hysteresis will lag what would have been the gain without hysteresis by P steps as register ADDR_A is ramping down and Q steps as register ADDR_A is ramping up. The rule in Case 1 allows for relaxation of the hysteresis when ADDR_A reaches a terminal value.

ROM SPL

In general, table ROM_SPL has N entries ($N = 2^n$). Even though the actual number of physical entries may be somewhat smaller than this power-of-two number, the address bus of ROM_SPL is n bits wide. The wordlength K of the SPL values are large enough so that adjacent SPL levels can be accurately distinguished. In one definition, if the entry number 0 (address 0) is the location where the SPL value just above the knee-SPL value is stored, register ADDR_A contains the exact address pointing to ROM_CSD. If, on the other hand, the entry number 0 (address 0) is the very location storing the knee-SPL value, the actual address pointing to ROM_CSD becomes (ADDR_A-1), and this definition is used in our design examples. Furthermore, the discrete SPL values (always positive numbers) increase monotonically with increment of the ROM address, whereas the gain values in ROM_CSD deceases monotonically.

Normally, the discrete SPL values stored in ROM_SPL can either be uniformly or non-uniformly distributed. But in this design non-uniformly distribution is more suitable since a CSD gain multiplier is used. (The magnitude distribution of CSD numbers is inherently non-uniform.) Thus, with non-uniform distribution of the discrete SPL values the maximally allowed step size on gain steps can be imposed so that the new digital AGC can achieve an equal or even better performance compared with digital AGCs having uniform gain steps. In practice 0.25 or 0.5-dB maximum gain step sizes are considered excellent and are used in the following design examples.

ROM CSD

CSD coding of binary numbers is an efficient way of performing multiplication operations. For example, a 16-bit binary number (including one sign bit) of c=0.100111001111101 equals to a sum of ten power-of-two items:

$$c = 2^{-1} + 2^{-4} + 2^{-5} + 2^{-6} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12} + 2^{-13} + 2^{-15} \quad (1)$$

When c is involved in a multiply operation there is a need of performing ten shifts and nine adds. The CSD coding on c gives:

$$c = 2^{-1} + 2^{-3} - 2^{-6} + 2^{-8} - 2^{-13} + 2^{-15} \quad (2)$$

Using CSD coding as in equation (2) a multiply now degenerates to just six shifts and five adds/subtracts. To further reduce shift 6 operations, c can be expressed in a nested form as:

$$c = 2^{-1} (1 + 2^{-2} (1 - 2^{-3} (1 - 2^{-2} (1 - 2^{-5} (1 - 2^{-2}))))) \quad (3)$$

Or c can be described as an even more efficient, nested multiplicative form:

$$c = 2^{-1} (1 + 2^{-2} (1 - 2^{-3} (1 - 2^{-2}) (1 + 2^{-7}))) \quad (4)$$

Now, a total of only four adds/subtracts are required in a multiply.

Either equation (3) or (4) may be employed to perform CSD coding of gain values in the new AGC design. Before going further, an additional constraint related to the maximally allowed shift bits is added. If the shift operation is hard wired, then no constraint need to be considered. But if the shift operation is based on a programmable shift circuitry, a limitation on the maximum shift bits in equations (3) and (4) is applied to further reduce hardware requirement.

Some more generalized expressions are now provided for efficient CSD coding in the new digital AGC as follows:

$$c = 2^{s}(1 \pm 2^{-\alpha} \pm 2^{-\beta}) \quad (5)$$

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$$c = 2^s(1 \pm 2^{-\alpha} \pm 2^{-\beta} \pm 2^{-\gamma}) \qquad (6)$$

$$c = 2^s(1 \pm 2^{-\alpha})(1 \pm 2^{-\beta}) \qquad (7)$$

$$c = 2^s(1 \pm 2^{-\alpha} \pm 2^{-\beta})(1 \pm 2^{-\gamma}) \qquad (8)$$

where s is an integer, and α, β and γ are positive integers. When implementing CSD multipliers by using any of equations (5-8), nested multiply structure equations (3) or (4) is usually more efficient and less noisy. On the other hand, equations (7) and (8) might slightly be more efficient than using equations (5) and (6) for CSD coding. In the design examples described in the next section, it is suggested to use equation (7) for cases with the maximum gain step size of 0.5 dB and equation (8) for those having gain steps less than 0.25 dB. Moreover, constraint is imposed on the maximally allowed shift bits whenever programmable shift circuitry is required.

A novel technique for reducing the ROM size of gain values is to build a large ROM by reusing a small one. This can be done when the gain values are divided into several blocks and these blocks contain identical numbers except that they are scaled by different power-of-two digits. For example, if V denotes a vector of 16 elements (gain values) and the first and last elements of V meet a so-called circling condition. To be specific, the circling condition suggests that the ratio of the value of the first element of V over twice the value of the last element of V be less than 1, and this ratio be within a range bounded by the maximum gain step. Then, a 64-element vector can be built (a total of 64 gain values) by concatenating four 16-element vectors: 2^3V, 2^2V, 2^1V and 2^0V. In doing so we don't have to actually erect a 64-word ROM with a 6-b address bus. Instead, only a 16-word ROM with 4-b address, achieving a 75% size-reduction compared to that of a 64-word ROM, is now implemented. The four different simple scale operations controlled by the remaining two address bits can easily be incorporated into a CSD multiplier.

CSD Multiplier

A CSD multiplier 20 shown in Figure 2 based on CSD coding of equations (5-8) is very simple in its hardware implementation.

Design Example #1

0. 5-dB-Gain-Step Cases

In both design examples a simple compression function is used and it has three regions. The first region is called a linear region where no compression is performed. The third is a saturated region where the gain is fixed (minimal). Between these two regions is a linearly compressed region and we now assume a 64-word ROM_SPL that stores discrete SPL values is already in place. Therefore, we have M=N=64 and n=6. (The value of K is tied to the accuracy of the stored SPL values.)

Now consider using the CSD coding of equation (7) to build ROM_CSD that follows the requirement of having the maximum gain step of 0.5dB. After studying the magnitude distribution of power-of-two digits and their combinations expressed in equation (7) a conclusion is reached on selecting the range of parameters s, α and β as: s={0,1}, α={3,4,5,6} and β={2,3,4,5}. It is obvious a CSD coding of L=7 bits is needed for s, α and β (1-b for s, two sets of 2-b for the shift and two 1-b for either an add or subtract).

The advantages of the above selections for those parameters include a highly efficient CSD coding as well as relative ease in picking gain values. For a range of 6 dB gain (a gain factor of 2), a total of 12 or more gain values are needed to insure gain steps no bigger than 0.5 dB. After careful investigating, a total of 16 basic gain values (elements of V) are chosen and are summarized in Table 1:

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Table 1: 16 Basic Gain Values of V in Design Example 1.

Addr	CSD-Form	Gain	Gain Step
0	$2^1(1 + 2^{-6})(1 - 2^{-4})$	1.904	-0.417dB
1	$2^1(1 - 2^{-5})(1 - 2^{-4})$	1.816	-0.410dB
2	$2^1(1 - 2^{-6})(1 - 2^{-3})$	1.723	-0.460dB
3	$2^1(1 - 2^{-4})(1 - 2^{-3})$	1.641	-0.424dB
4	$2^1(1 + 2^{-4})(1 - 2^{-2})$	1.594	-0.252dB
5	$2^1(1 + 2^{-6})(1 - 2^{-2})$	1.523	-0.392dB
6	$2^1(1 - 2^{-5})(1 - 2^{-2})$	1.453	-0.410dB
7	$2^0(1 + 2^{-3})(1 + 2^{-2})$	1.406	-0.285dB
8	$2^0(1 + 2^{-4})(1 + 2^{-2})$	1.328	-0.496dB
9	$2^0(1 + 2^{-3})(1 + 2^{-3})$	1.266	-0.419dB
10	$2^0(1 + 2^{-4})(1 + 2^{-3})$	1.195	-0.496dB
11	$2^0(1 + 2^{-5})(1 + 2^{-3})$	1.160	-0.259dB
12	$2^0(1 + 2^{-4})(1 + 2^{-4})$	1.129	-0.237dB
13	$2^0(1 + 2^{-6})(1 + 2^{-4})$	1.079	-0.392dB
14	$2^0(1 + 2^{-6})(1 + 2^{-5})$	1.047	-0.259dB
15	$2^0(1 - 2^{-5})(1 + 2^{-5})$	0.999	-0.410dB

Notice that the gain step of -0.417 dB at Addr 0 is evaluated based on the very previous gain value of $2^1(1 - 2^{-5})(1 + 2^{-5})$ that is exactly two times of the last gain value at Addr 15 in Table 1. Such an intentionally designed feature is the previously-described circling condition that makes a catenating of more than one vectors realizable. The

maximum gain step of V (and its catenated expansion vector as well) is 0.496 dB while the minimum is just 0.237 dB.

As expected, four vectors of 2^3V, $2^2 V$, 2^1V and 2^0V can be easily catenated into a 64-entry vector. A 16-word ROM storing the gain values of V is built because the address generated by the state machine is of 6-bits, the four LSBs address this 16-word ROM whereas the two MSBs are relayed to a CSD multiplier to perform a simple scale (shift) operation.

A very efficient CSD multiplier implementing equation on (7) plus a shift

related to four scale (2^0 to 2^3) operations is depicted in Figure 2. α and β (3b) control 4 shifts and one add/subtract whereas s and the two MSBs of the address selects a multi-bit shift from 0 to 7 bits.

Design Example #2

0.25-dB-Gain-Step Cases

Similar to the first design example, it is assumed M=N=64 and n=6, but equation (8) is now employed to code gain values that have gain steps smaller than 0.25 dB step. Empirical knowledge indicates that parameters s, α, β and γ in equation (8) may be configured as: s={2,3}, α ={3,4,5,6} and γ={2,3,4,5}, and β is an integer larger than α but which cannot exceed α+4. Therefore, a CSD code for a gain value is L=10 bits (1-b for s, 3-b for α, 3-b for β, and 3-b for γ).

Without much difficulty, 32 possible gain values can be picked and coded based on equation (8) and are summarized in Table 2.

Notice that the largest gain step in this design example is 0.243 dB and the minimum step is just 0.123 dB. Based on the circling condition described before, the first gain step of -0.178 dB should be a downward deviation from the gain value of $2^3(1 - 2^{-5}(1 + 2^{-3}))(1 + 2^{-5})$, which without surprise is twice the magnitude of the last gain in V of Table 2.

Table 2: 32 Basic Gain Values of V in Design Example 2.

Addr	CSD-Form	Gain	Gain Step
0	$2^3(I - 2^{-4}(I - 2^{-3}))(1 + 2^{-5})$	7.799	-0.178dB
1	$2^3(I - 2^{-4}(I + 2^{-2}))(1 + 2^{-5})$	7.605	-0.218dB
2	$2^3(I - 2^{-5}(I + 2^{-2}))(1 - 2^{-5})$	7.295	-0.180dB
3	$2^3(I - 2^{-5}(I - 2^{-3}))(1 - 2^{-4})$	7.295	-0.180dB
4	$2^3(I - 2^{-5}(I + 2^{-1}))(1 - 2^{-4})$	7.148	-0.176dB
5	$2^3(I - 2^{-4}(I + 2^{-4}))(1 - 2^{-4})$	7.002	-0.180dB
6	$2^3(I - 2^{-5}(I - 2^{-2}))(1 - 2^{-3})$	6.836	-0.208dB
7	$2^3(I - 2^{-5}(I + 2^{-1}))(1 - 2^{-3})$	6.672	-0.211dB
8	$2^3(I - 2^{-4}(I + 2^{-4}))(1 - 2^{-3})$	6.535	-0.180dB
9	$2^3(I + 2^{-4}(I + 2^{-4}))(1 - 2^{-2})$	6.398	-0.184dB
10	$2^3(I + 2^{-4}(I - 2^{-2}))(1 - 2^{-2})$	6.281	-0.161dB
11	$2^3(I + 2^{-5}(I - 2^{-2}))(1 - 2^{-2})$	6.141	-0.197dB
12	$2^3(I + 2^{-6}(I - 2^{-1}))(1 - 2^{-2})$	6.047	-0.134dB
13	$2^2(I + 2^{-3}(I + 2^{-1}))(1 + 2^{-2})$	5.938	-0.159dB

14	$2^2(I + 2^{-3}(I + 2^{-2}))(1 + 2^{-2})$	5.781	-0.232dB
15	$2^2(I + 2^{-3}(I + 2^{-4}))(1 + 2^{-2})$	5.664	-0.178dB
16	$2^2(I + 2^{-3}(I - 2^{-3}))(1 + 2^{-2})$	5.547	-0.182dB
17	$2^2(I + 2^{-4}(I + 2^{-1}))(1 + 2^{-2})$	5.469	-0.123dB
18	$2^2(I + 2^{-4}(I + 2^{-2}))(1 + 2^{-2})$	5.391	-0.125dB
19	$2^2(I + 2^{-4}(I - 2^{-3}))(1 + 2^{-2})$	5.273	-0.191dB
20	$2^2(I + 2^{-5}(I - 2^{-3}))(1 + 2^{-2})$	5.137	-0.228dB
21	$2^2(I + 2^{-6}(I - 2^{-1}))(1 + 2^{-2})$	5.039	-0.167dB
22	$2^2(I - 2^{-6}(I + 2^{-2}))(1 + 2^{-2})$	4.902	-0.239dB
23	$2^2(I - 2^{-5}(I + 2^{-2}))(1 + 2^{-2})$	4.805	-0.175dB
24	$2^2(I - 2^{-4}(I - 2^{-4}))(1 + 2^{-2})$	4.707	-0.178dB
25	$2^2(I + 2^{-5}(I - 2^{-2}))(1 + 2^{-3})$	4.605	-0.189dB
26	$2^2(I + 2^{-4}(I - 2^{-4}))(1 + 2^{-4})$	4.499	-0.203dB
27	$2^2(I + 2^{-5}(I + 2^{-3}))(1 + 2^{-4})$	4.399	-0.194dB
28	$2^2(I + 2^{-6}(I - 2^{-2}))(1 + 2^{-4})$	4.300	-0.199dB
29	$2^2(I + 2^{-5}(I - 2^{-1}))(1 + 2^{-5})$	4.189	-0.226dB
30	$2^2(I - 2^{-6}(I - 2^{-1}))(1 + 2^{-5})$	4.093	-0.203dB
31	$2^2(I - 2^{-5}(I + 2^{-3}))(I + 2^{-5})$	3.980	-0.243dB

To build an equivalent 64-word ROM a 32-word ROM the 5 LSBs can be employed as the address bus, and the MSB of the 6-b address is fed into a CSD multiplier where an additional 1-bit programmable shift is added.

The CSD multiplier 20 in this example needs one more shift and one more add (subtract) when compared with that in Design Example 1 (see Figure 2); therefore, the small gain steps can be achieved by using an efficient hardware implementation.

An efficient digital AGC system has been disclosed. New features achieve an efficient design, having novel advantageous properties summarized as follows:

1. A simple state machine consisting of two comparators and several registers is employed to locate the corresponding gain value based on a current measure of the peak level of the input signals. While one ROM table stores the gain values, the other contains the discrete SPL peak values.

2. The gain values are coded in CSD forms, and as a result the gain multiplier degenerates to just a couple of shift and add operations. The various CSD coding forms for this purpose have been expounded by equations (2-8).

3. A small portion of the gain values can be selected such that they satisfy the circling condition. The design examples illustrate how to reuse a small ROM to build an equivalent large ROM under this condition. The saving on the gain value ROM can be up to 75%.

GROUNDS OF REJECTION

The two grounds of rejection are first whether Claims 3, 4, 6, 7, 10, 25-28, and 31 are unpatentable under 35 U.S.C. § 103 over Wilson in view of Hausman and Lee; and second whether Claim 15 is unpatentable over Smart in view of Dallavalle.

ARGUMENTS

Applicant respectfully submits that the rejection of Claim 15 is obviates by the cancellation of this claim.

It is respectfully submitted that Wilson does not disclose or suggest the presently claimed invention including the automatic gain control circuit wherein the gain includes a canonical sign digit multiplier in independent Claims 3, 4, and 7 albeit defined as the method step of providing automatic gain control to the input signal wherein the gain is applied by a canonical signed multiplier in independent Claims 25 and 28.

Applicants agree with the Examiner that Wilson does not disclose the CSD multiplier.

It is respectfully submitted that Hausman does not disclose or suggest the automatic gain control circuit wherein the gain includes a canonical signed digit multiplier in the various forms in independent Claims 3, 4, 7, 25, and 28.

Hausman does not disclose an ADC as presently claimed and does not disclose that it would be used with an ADC. Hausman is an improper reference.

The Examiner has used impermissible hindsight in this rejection.

Lee does not disclose a canonical signal digital multiplier in an ADC.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 3, 4, 6, 10, 25-28, and 31 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Appellants
Reg. No. 34,478

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-5633

APPENDIX

Claims 1 and 2 (cancelled)

Claim 3 (previously presented): An automatic gain control (AGC) circuit, comprising:

an input adapted to receive a signal;

a compression circuit coupled to the input having a compression ratio, the compression ratio being applied to the signal exceeding a first predetermined threshold, the compression ratio being applied as a function of a predetermined signal peak level,

wherein said circuit further comprises a gain applied to the signal, which gain is not uniformly distributed to the signal, and

wherein the gain comprises a canonical signed digit (CSD) multiplier.

Claim 4 (previously presented): An automatic gain control (AGC) circuit, comprising:

an input adapted to receive a signal;

a compression circuit coupled to the input having a compression ratio, the compression ratio being applied to the signal exceeding a first predetermined threshold, the compression ratio being applied as a function of a predetermined signal peak level,

wherein said circuit further comprises a gain applied to the signal, which gain is not uniformly distributed to the signal, and

wherein the gain comprises a canonical signed digit (CSD) multiplier,

wherein a maximum gain step of the gain is between 0.25 and 0.5dB.

Claim 5 (cancelled).

Claim 6 (original): The automatic gain control circuit as specified in Claim 3 wherein the CSD multiplier adjusts the gain in real time.

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Claim 7 (currently amended): An automatic gain control (AGC) circuit, comprising:

an input adapted to receive a signal;

a compression circuit coupled to the input having a compression ratio, the compression ratio being applied to the signal exceeding a first predetermined threshold, the compression ratio being applied as a function of a predetermined signal peak level,

wherein said circuit further comprises a gain applied to the signal, which gain is not uniformly distributed to the signal,

wherein the gain comprises a canonical signed digit (CSD) multiplier; and

a look-up table storing discrete sound pressure level (SPL) values and a second table storing information indicative of gain values.

Claim 8 (original): The automatic gain control circuit as specified in Claim 7 further comprising a state machine tracking a peak level of the signal such that positions of an upper and lower SPL value is determined in one table.

Claim 9 (original): The automatic gain control circuit as specified in Claim 8 wherein the gain value in the second table is a function of the state machine tracking.

Claim 10 (original): The automatic gain control circuit as specified in Claim 7 wherein the second table stores CSD codes rather than actual gain values.

Claim 11 (original): The automatic gain control circuit as specified in Claim 10 further comprising a table storing only a fraction of actual gain values.

Claim 12 (original): The automatic gain control circuit as specified in Claim 11 wherein remaining actual gain values are determined by a scale factor.

Claim 13 (original): The automatic gain control circuit as specified in Claim 12 wherein the scale factor is a 2^S scale factor.

Claim 14 (original): The automatic gain control circuit as specified in Claim 12 wherein the scale factor is a simple shift.

Claim 15 (previously presented): An automatic gain control (AGC) circuit, comprising:

an input adapted to receive a signal;

a compression circuit coupled to the input having a compression ratio, the compression ratio being applied to the signal exceeding a first predetermined threshold, the compression ratio being applied as a function of a predetermined signal peak level,

wherein the compression circuit comprises a state machine having a first and second comparator and a first and second register, the first comparator comparing the input signal to the content of the first register and the second comparator comparing the input signal to the content of the second register.

Claim 16 (previously presented): An automatic gain control (AGC) circuit, comprising:

an input adapted to receive a signal;

a compression circuit coupled to the input having a compression ratio, the compression ratio being applied to the signal exceeding a first predetermined threshold, the compression ratio being applied as a function of a predetermined signal peak level,

wherein the compression circuit comprises a state machine having a first and second comparator and a first and second register, the first comparator comparing the input signal to the content of the first register and the second comparator comparing the input signal to the content of the second register,

wherein the content of the first register is moved to the second register when the input signal exceeds the first predetermined threshold.

Claim 17 (original): The automatic gain control circuit as specified in Claim 16 further comprising a third and fourth register, wherein the content of the third register is also responsively moved to the fourth register and the content of the third register is decreased by 1.

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Claim 18 (original): The automatic gain control circuit as specified in Claim 2 3 wherein the gain has hysteresis.

Claim 19 (original): The automatic gain control circuit as specified in Claim 7 wherein the SPL values are uniformly distributed.

Claim 20 (original): The automatic gain control circuit as specified in Claim 7 wherein the SPL values are not uniformly distributed.

Claim 21 (original): The automatic gain control circuit as specified in Claim 11 wherein the gain values are divided into blocks of numbers, the blocks being scaled with respect to each other.

Claim 22 (original): The automatic gain control circuit as specified in Claim 21 wherein the scaling of blocks is by a power-of-two.

Claims 23 and 24 (cancelled).

Claim 25 (previously presented): A method of providing automatic gain control (AGC) to an input signal, comprising the steps of:
    providing a compression ratio to the input signal when the input signal exceeds a first predetermined threshold; and
    applying a gain to the input signal, wherein the gain is not uniformly distributed to the signal,
    wherein the gain is applied by a canonical signed digit (CSD) multiplier.

Claim 26 (original): The method as specified in Claim 25 wherein the gain is applied after evaluating the compression ratio.

Claim 27 (original): The method as specified in Claim 25 wherein the CSD multiplier adjusts the gain in real time.

Claim 28 (previously presented): A method of providing automatic gain control (AGC) to an input signal, comprising the steps of:

providing a compression ratio to the input signal when the input signal exceeds a first predetermined threshold; and

applying a gain to the input signal, wherein the gain is not uniformly distributed to the signal,

wherein the gain is applied by a canonical signed digit (CSD) multiplier,

a look-up table storing discrete sound pressure level (SPL) values and a second table storing information indicative of gain values.

Claim 29 (original): The method as specified in Claim 28 further comprising a state machine tracking a peak level of the signal such that positions of an upper and lower SPL value is determined in one table.

Claim 30 (original): The method as specified in Claim 29 wherein the gain value in the second table is a function of the state machine tracking.

Claim 31 (original): The method as specified in Claim 25 wherein the second table stores CSD codes rather than actual gain values.

Claim 32 (original): The method as specified in Claim 31 further comprising a table storing only a fraction of actual gain values.

Claim 33 (original): The method as specified in Claim 32 wherein remaining actual gain values are determined by a scale factor.

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EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.